Locally Strained Ultra-Thin Channel 25 nm Narrow FDSOI Devices with Metal Gate and Mesa Isolation

Z. Krivokapič, V. Moroz*, W. Maszara, M.-R. Lin,

AMD, Technology Research Group

*Synopsys

Outline

- **Motivation**
- Device Fabrication
- Experimental Data
- Simulation Results
- Conclusions

Motivation

- In order to achieve goals in the ITRS roadmap, performance enhancements are needed
- Uniformly strained channels offer significant mobility enhancement but they scale unfavorably with smaller L and/or W — Q. Xiang et al, VLSI 2003
- Narrow ultra thin FDSOI devices show very good DIBL and lower off-state leakage — Z. Krivokapic et al, SSDM 2003
- A straining approach that scales well with smaller W and L

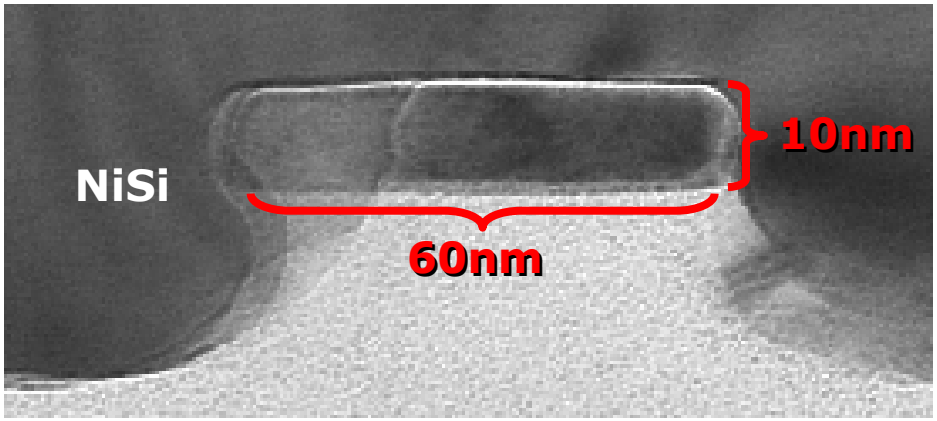
Outline

- Motivation
- **Device Fabrication**
- Experimental Data
- Simulation Results
- Conclusions

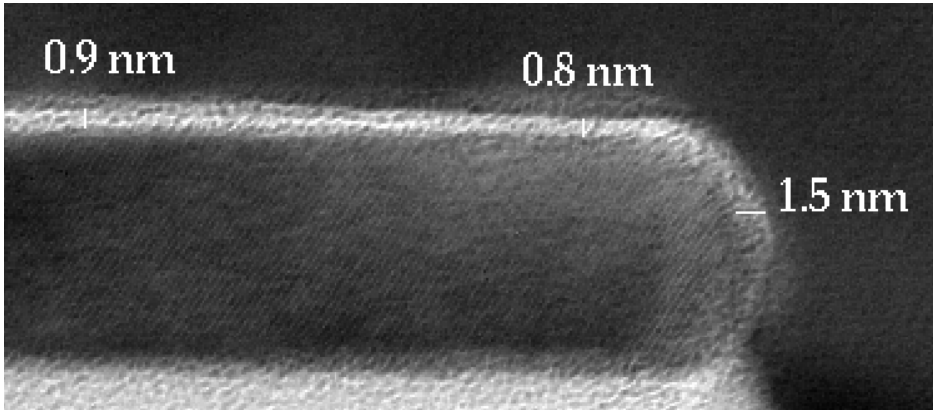
Device Fabrication

- SOI wafer with 200nm buried oxide is thinned to sub-10nm thickness
- Mesa isolation is used for simplicity
- Nitrided oxide with Tox,inv = 1.5nm is used
- The polysilicon gate wraps the channel from three sides
- After very thin nitride spacer (<15nm) we grow 30nm of selective epitaxial silicon
- After source/drain formation and planarization the polysilicon gates are fully silicided to form a mid-gap work function gate

Very Narrow Channel



Total channel width is 60nm + 2*10nm = 80nm

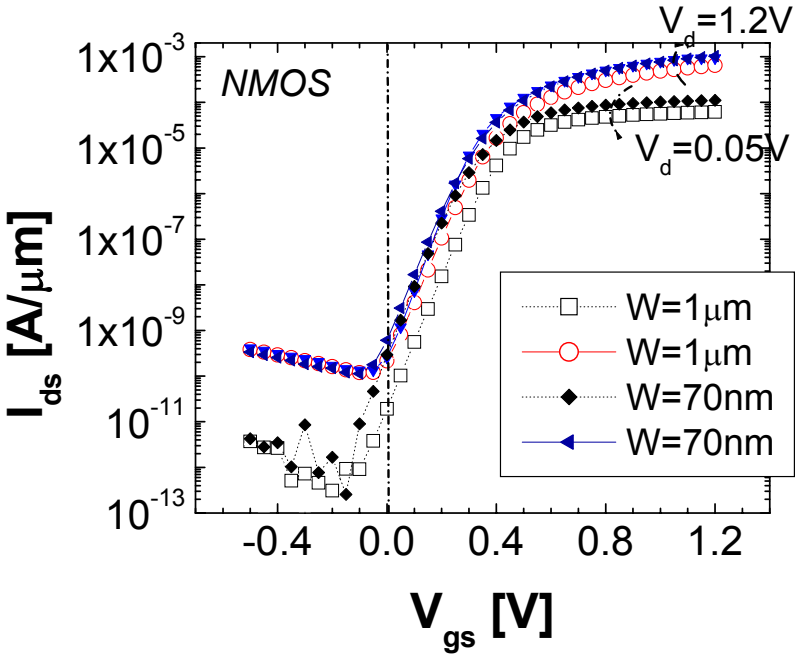


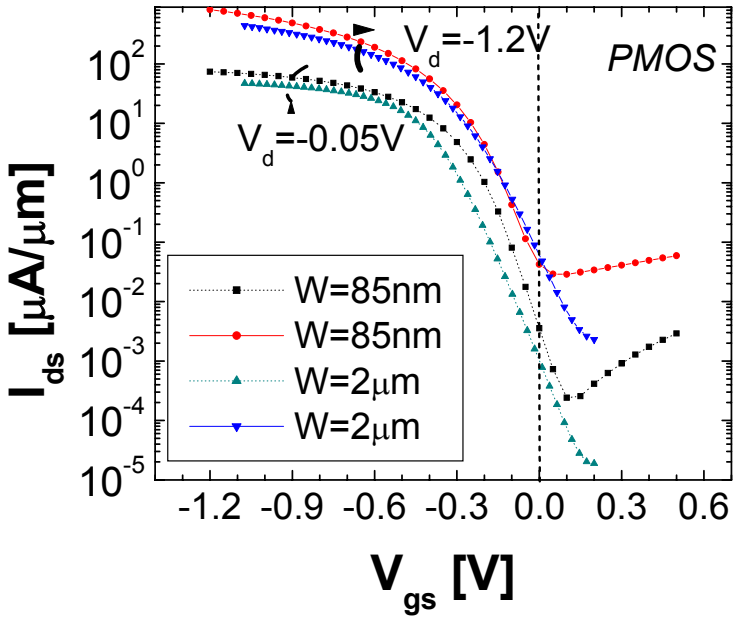
Gate dielectric is thinner at the corner but thickens on the sidewalls

Outline

- Motivation
- Device Fabrication
- **Experimental Data**
- Simulation Results
- Conclusions

Ids – Vgs for 25nm Devices





Narrow devices show better DIBL and larger I_{on}

Devices with Different Width

L_{gate}~ 25nm

NMOS

W (nm)	DIBL (mV/V)	I_{on} (mA/μm)
80	18	1.033
130	30	0.742
1000	52	0.649

I_{off}~ 0.2-0.6 nA/μm

@V_{dd} = 1.2V

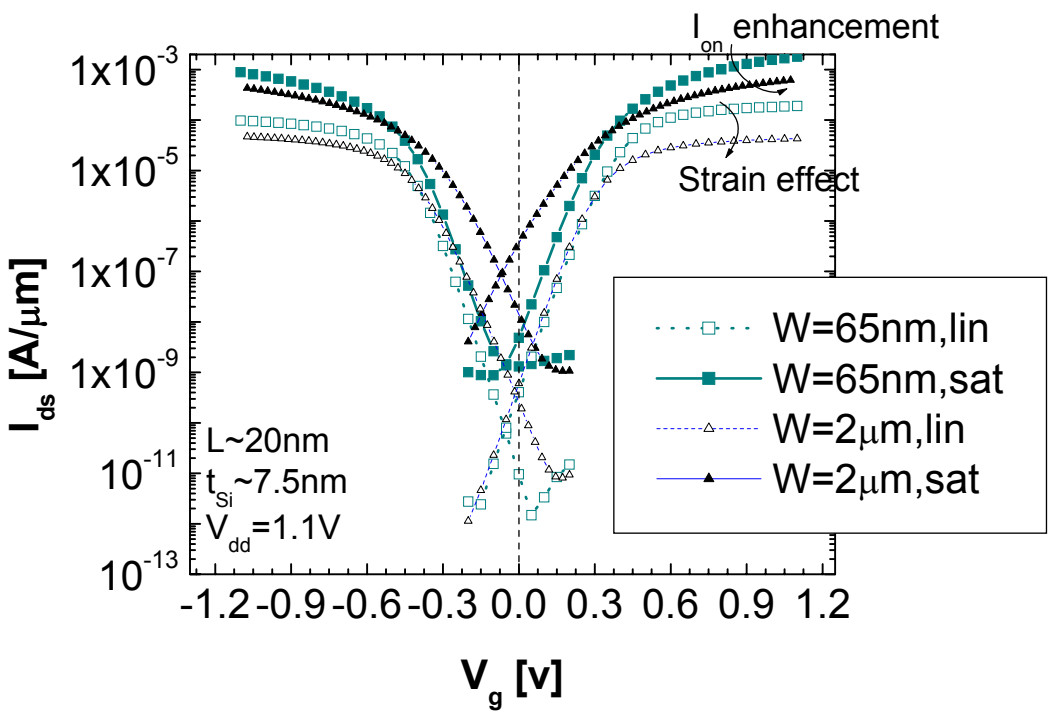
PMOS

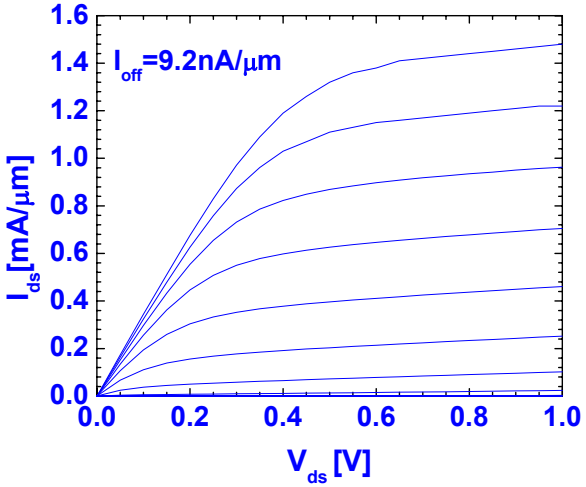
W (nm)	DIBL (mV/V)	I_{on} (mA/μm)
80	52	896
125	91	685
2000	167	589

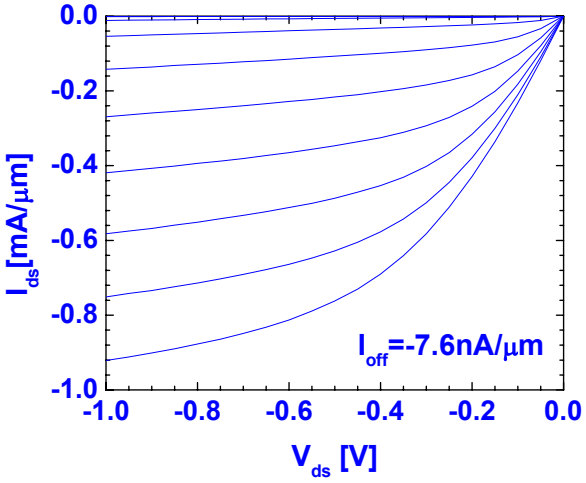
I_{off}~ 200-300 nA/μm

@V_{dd} = 1.2V

20nm Narrow Devices





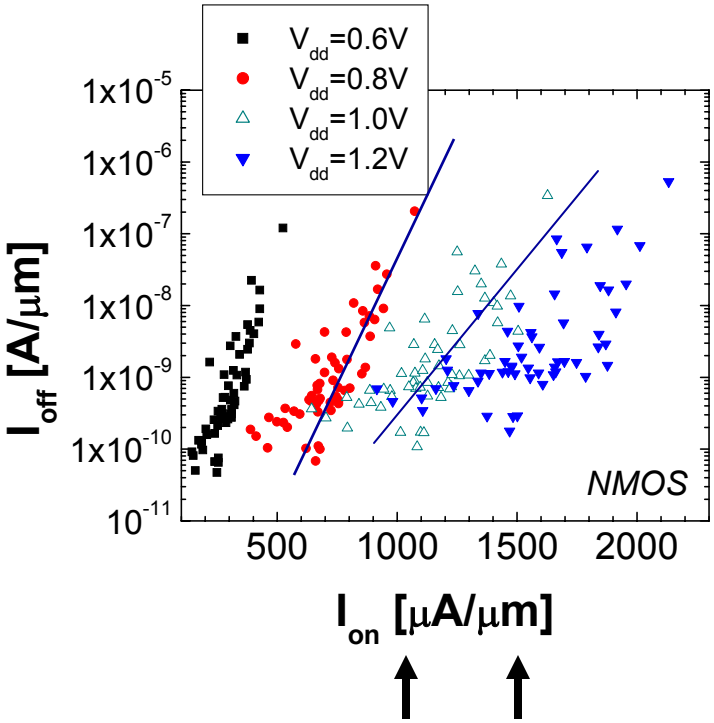


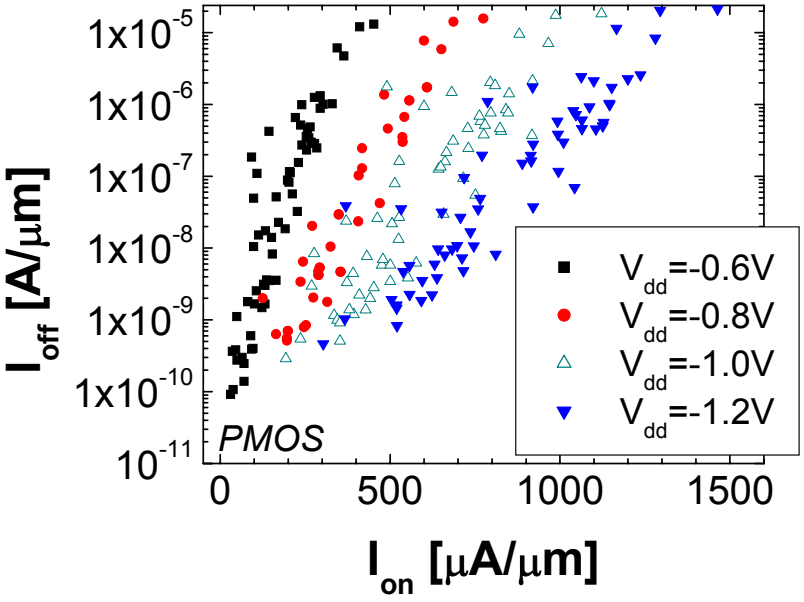
Narrow NMOS devices show much better I_{off}

20nm Devices

Device Parameter	NMOS	PMOS
L_{gate} [nm]	20	20
$T_{ox,inv}$ [nm]	1.7	1.7
I_{on} [mA/μm] @V_{dd}=1V	1.47	0.94
I_{off} [nA/ μm] @V_{dd}=1V	9.2	7.6
S [mV/dec]	73.1	72.3
DIBL [mv/V]	85	90
CV/I [ps]	0.24	0.43

I_{on} vs. I_{off} for Narrow Devices



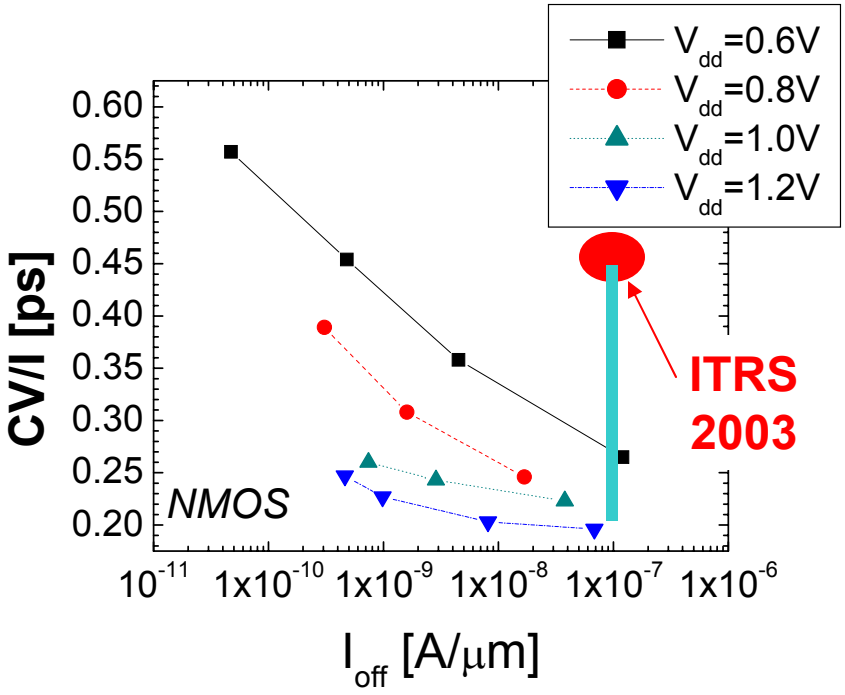


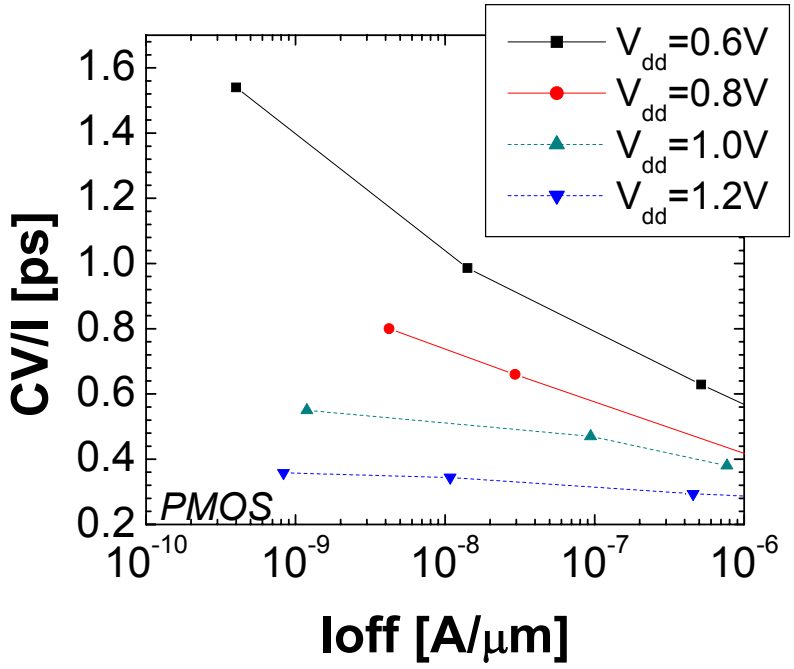
I_{on}~1.1mA/μm for
I_{off}=1μA/μm @ V_{dd}=0.8V

I_{on}~1.5mA/μm for
I_{off}=70nA/μm @ V_{dd}=1.0V

PMOS devices have too strong extension dose

CV/I



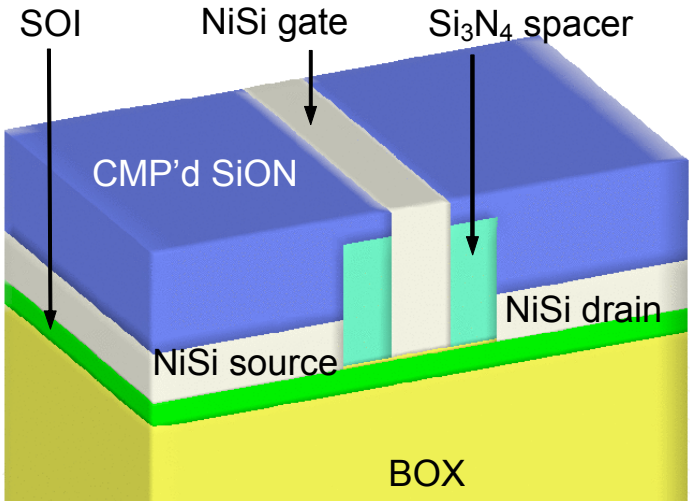


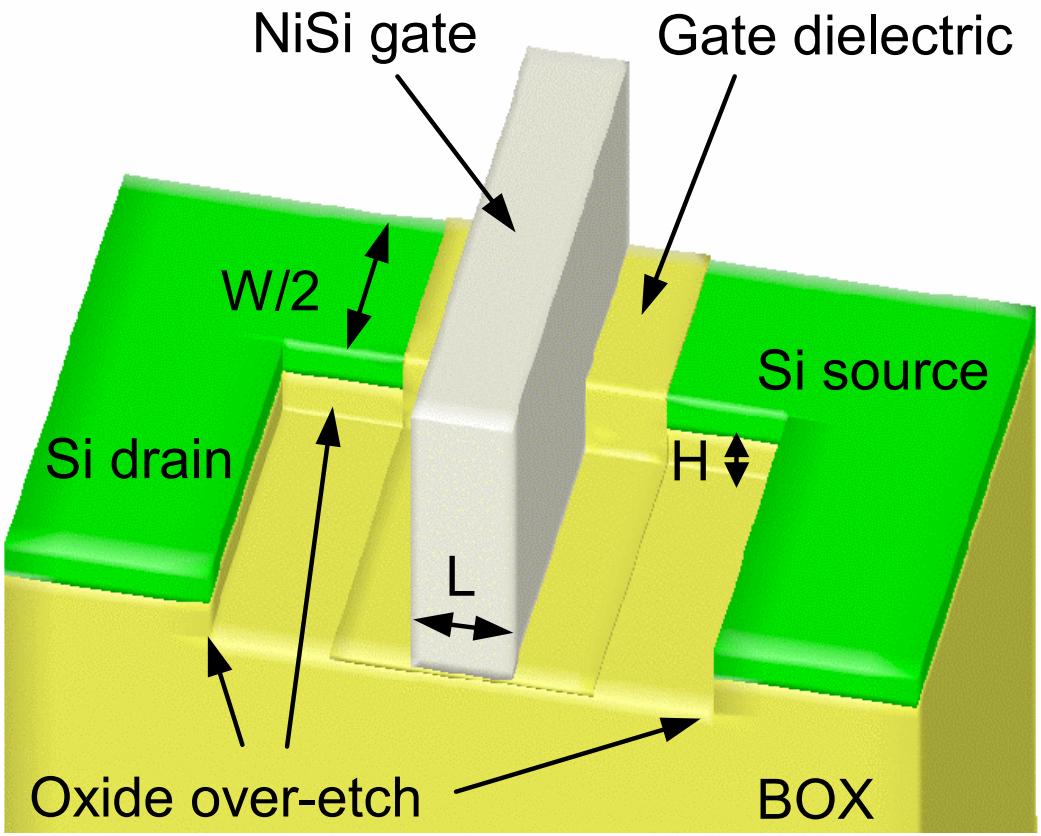
>2x Improvement in CV/I

Outline

- Motivation
- Device Fabrication
- Experimental Data
- **Simulation Results**
- Conclusions

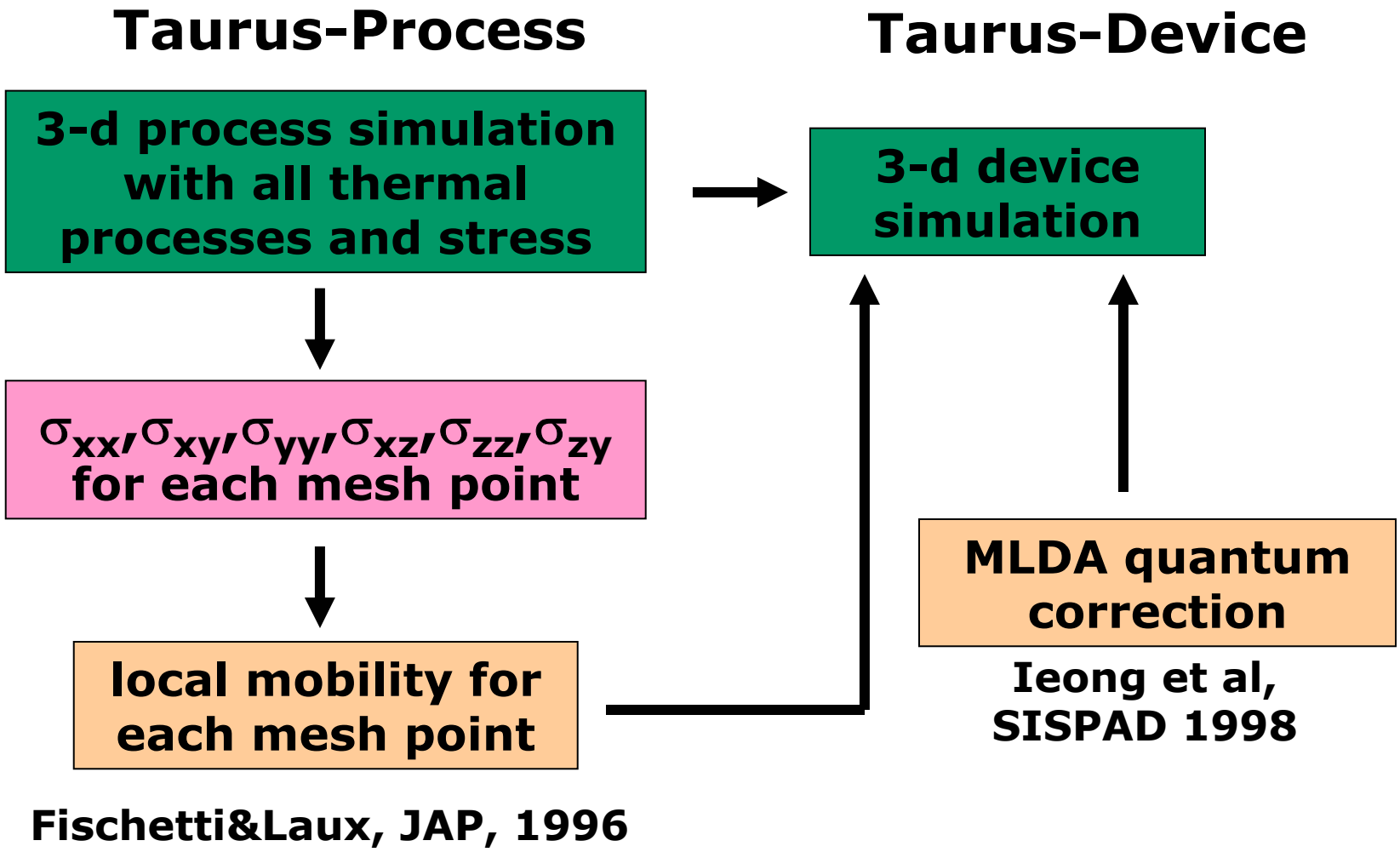
Simulation Structure



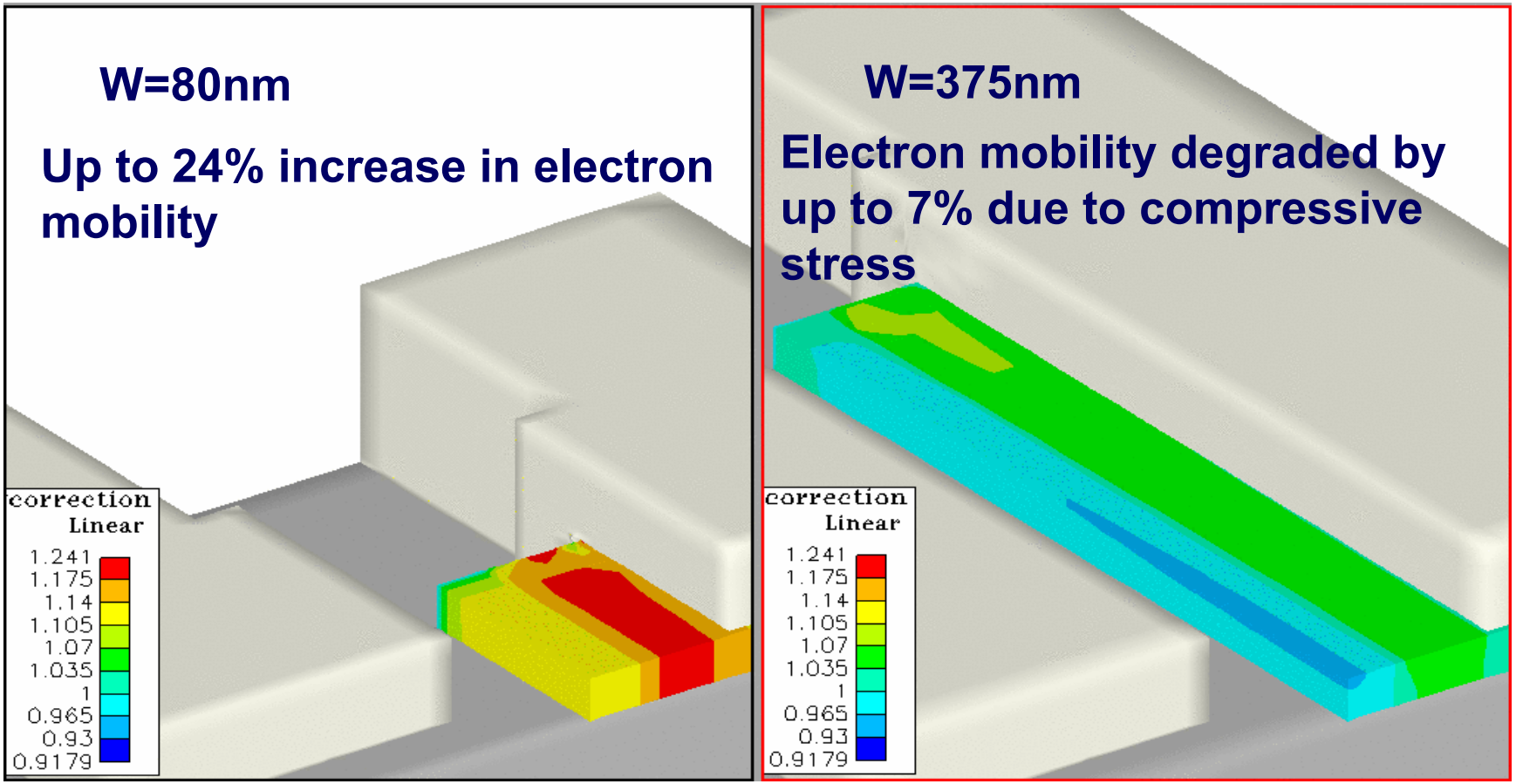


Half-width of a 25nm transistor without selective epi

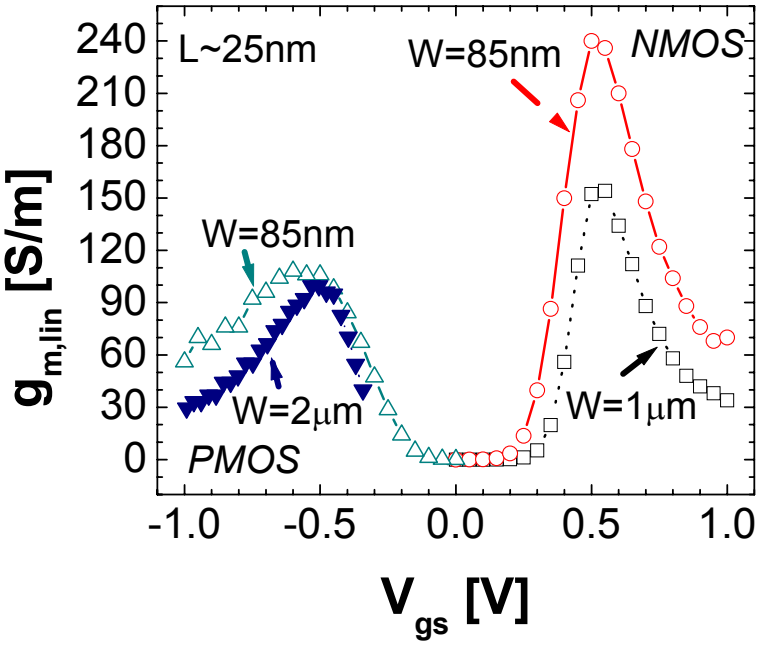
Simulation Methodology



Local Mobility for Different W



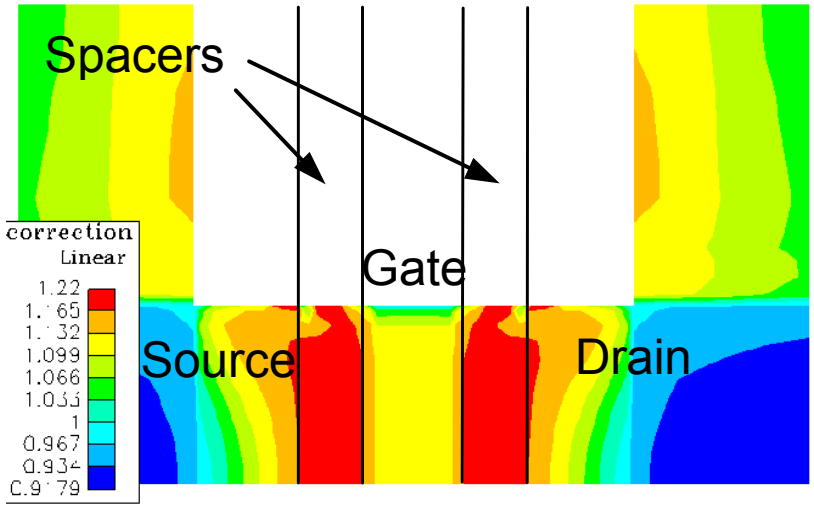
Change in Strain

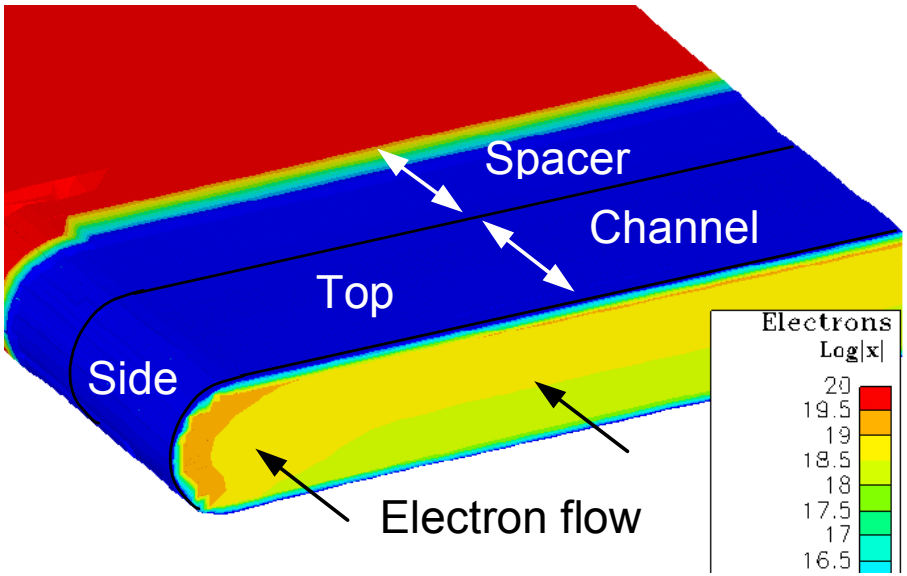


NMOS linear transconductance increases dramatically because the strain for narrow devices becomes tensile, while for wider devices it is compressive

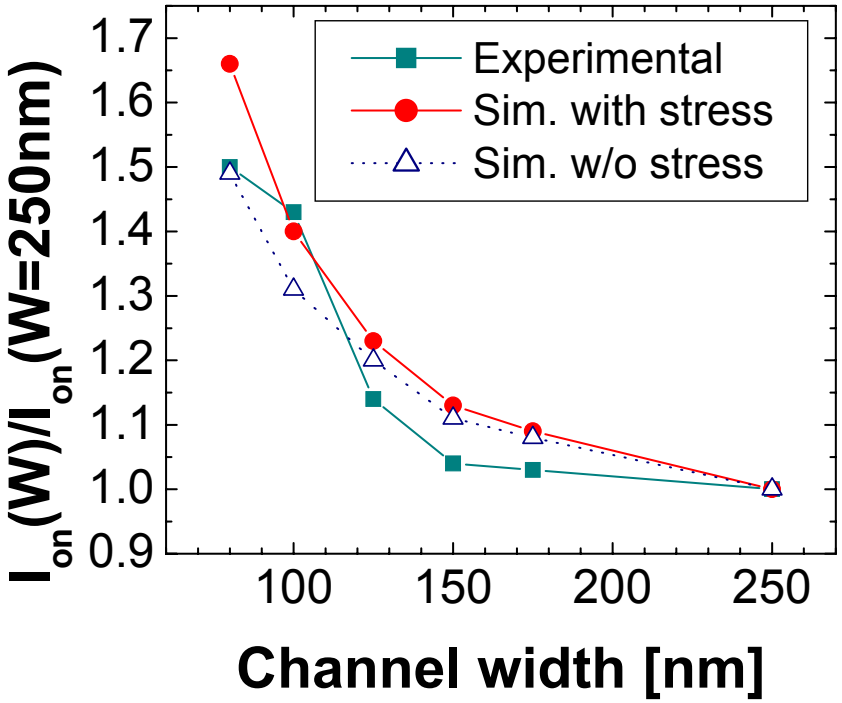
Local Mobility and Current Flow

- **Mobility enhancement changes locally**
- **Larger inversion charge on the sidewalls**
- **Large amount of current doesn't flow through the area of largest mobility enhancement**





Drive Current vs. NMOS Width

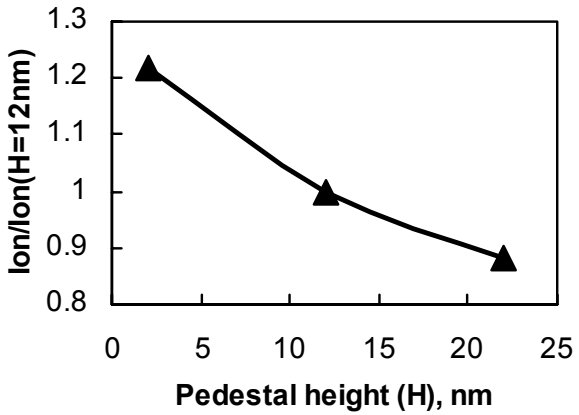


- **Simulation results reproduce empirical trend**
- **For narrow devices (~75nm) 30% of current enhancement comes from local strain**

Critical Processes for Localized Strain

- Intrinsic stress in the metal gate, spacers, and silicides are the dominant factors that determine local strain in the channel
- Silicon layer thickness and amount of buried oxide over-etch also change a lot

10nm increase in buried oxide over-etch results in 20% change in NMOS I_{on}.



Outline

- Motivation
- Device Fabrication
- Experimental Data
- Simulation Results
- **Conclusions**

Conclusions

- We demonstrate ultra thin FDSOI devices with mesa isolation and tensile FUSI metal gates with the record low CV/I
- Narrow devices in our process exhibit significant performance enhancement over wide ones
- Using 3-d simulations we reproduce experimental data
- We show that many processing steps can affect the local strain
- Optimization of local strain and electrostatics may yield very high performing devices

Acknowledgments

- New simulation modules development
  - **L. Smith**
- Characterization
  - **C. Volkman**
- TEM analysis
  - **J. Gray**

Trademark Attribution